A clean version of the claims is submitted below:

1. (currently amended) A semiconductor, comprising:

a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the wafer, such wafer having a plurality of electrical contacts;

a self-supporting dielectric member having an electrical conductor thereon, such electrical conductor being elevated above the regions in the fractional portion of the wafer, such electrical conductor being electrically connected to the plurality of electrical contacts to electrically interconnect such plurality of chips, portions of the dielectric member with portions of the electrical conductor thereon spanning the regions in the wafer; and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips.

3. (currently amended) The semiconductor recited in claim 1 wherein each one of the voltage generators is disposed in the separating region.

6. (currently amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

a self-supporting\g dielectric member having an electrical conductor thereon electrically connecting the plurality of electrical selected one or ones of the

electrical components to the chips with portions of the electrical conductor elevated above the regions in the fractional portion of the wafer and spanning the separating regions between the chips in the fractional portion of the wafer.

7. (previously amended) The semiconductor recited in claim 6 wherein each set of electrical components includes a plurality of different electrical components.

8. (withdrawn)

9. (withdrawn)

10. (previously amended) The semiconductor recited in claim 6 including

a fusible link electrically connecting a bus disposed in at least one of the plurality of integrated circuit chips and a corresponding one of the plurality of electrical components.

11. (currently amended) A semiconductor, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by separating regions in the fractional portion of the wafer;

a plurality of sets of electrical components, each set being associated with, and adjacent to, a corresponding one of the chips; and

an electrical conductor electrically connecting the plurality of electrical selected one or ones of the electrical components to the chips with portions of the electrical conductor elevated above the regions in the fractional portion of the wafer and spanning the separating regions between the chips in the fractional portion of the wafer; and

wherein each one of the electrical components is disposed in the separating region.

12. (previously added) The semiconductor recited in claim 11 wherein the electrical components are voltage generators.

13. (previously amended) The semiconductor recited in claim 12 wherein the voltage generators are interconnected by the conductor elevated above the regions in the fractional portion of the wafer.

14. (withdrawn)

15. (previously added) The semiconductor recited in claim 12 wherein at least one of the voltage generators is coupled to more than one bus in corresponding ones of the plurality of integrated circuit chips.

16. (currently amended) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

a self-supporting dielectric member having an electrical conductor thereon, such electrical conductor being electrically connected to the plurality of electrical contacts to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer; and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips.

17. (currently amended) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

a dielectric member having an electrical conductor thereon, such electrical conductor being electrically connected to the plurality of electrical contacts to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer; and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips; and

wherein each one of the voltage generators is disposed in the separating region.

18. (currently amended) A semiconductor package, comprising:

a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

a self-supporting dielectric member having an electrical conductor thereon electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer, such conductor being elevated above the regions in the fractional portion of the wafer; and

a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips.

19. (currently amended) The semiconductor package recited in claim 18 wherein each one of the voltage generators is disposed in the separating region.

20. (currently amended) A semiconductor packaging arrangement, comprising:

(A) a printed circuit board having an electrical interconnect thereon;

(B) a semiconductor package, comprising:

(i) a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

(ii) a self-supporting dielectric member having an electrical conductor thereon electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer; and

(iii) a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips; and

(C) a conductor for electrically connecting the electrical conductor of the package to the electrical interconnect of the printed circuit board.

21. (currently amended) A semiconductor packaging arrangement, comprising:

(A) a printed circuit board having an electrical interconnect thereon;

(B) a semiconductor package, comprising:

(i) a fractional portion of a semiconductor wafer having a plurality of integrated circuit chips thereon, such chips being separated by regions in the fractional portion of the wafer, such fractional portion of the wafer having a plurality of electrical contacts;

(ii) an electrical conductor electrically connected to the plurality of electrical contacts of the plurality of chips to electrically interconnect such

plurality of chips, portions of the electrical conductor spanning the regions in the fractional portion of the wafer; and

(iii) a plurality of voltage generators, each one being associated with, and disposed adjacent to, a corresponding one of the chips; and

(C) a conductor for electrically connecting the electrical conductor of the package to the electrical interconnect of the printed circuit board; and

wherein each one of the voltage generators is disposed in the separating region.

22. (new) The semiconductor recited in claim 1 wherein the self-supporting dielectric member is a printed circuit board.

23. (new) The semiconductor recited in claim 6 wherein the self-supporting dielectric member is a printed circuit board.

24. (new) The semiconductor package recited in claim 16 wherein the self-supporting dielectric member is a printed circuit board.

25 (new) The semiconductor package recited in claim 18 wherein the self-supporting dielectric member is a printed circuit board.

26. (new) The semiconductor packaging arrangement recited in claim 20 wherein the self-supporting dielectric member is a printed circuit board.